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(54) Title: SYSTEM AND METHOD FOR FABRICATING LOGIC DEVICES COMPRISING CARBON NANOTUBE TRANSISTORS

(57) Abstract: Carbon nanotube devices and methods for fabricating these devices, wherein in one embodiment, the fabrication process consists of the following process steps: (1) generation of a template, (2) catalyst deposition, and (3) nanotube synthesis within the template. In another embodiment, a carbon nanotube transistor comprises a carbon nanotube having two or more defects, wherein the defects divide the carbon nanotube into three regions having differing conductivities. The defects may be introduced by varying the diameter of a template in which the carbon nanotube is fabricated and thereby causing pentagon-heptagon pairs which form the defects.

DESCRIPTION

SYSTEM AND METHOD FOR FABRICATING LOGIC DEVICES COMPRISING CARBON NANOTUBE TRANSISTORS

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to logic devices and more specifically to a design, system, and method for fabricating logic devices comprising carbon nanotube molecular electronic devices.

BACKGROUND OF THE INVENTION

The U.S. semiconductor industry is facing increasingly difficult challenges as it moves into the production of features at sizes approaching 100 nanometers. The magnitude of some of these challenges has led to their being singled out as industry leaders as "grand challenges" requiring major initiatives to develop solutions using approaches with no historical precedent. Four of the six grand challenges identified in the National Technology Roadmap For Semiconductor include the ability to have affordable scaling, affordable lithography at and below 100 nanometers, new materials and structures, and gigahertz frequency operations on chips.

According to the technology roadmap for semiconductors, the minimum size of features will have to reach 130 nanometers by 2003 to keep pace with the continued doubling of the number of transistors on a chip every 18 months. After 2003, the roadmap indicates a lack of consensus about how to solve the fabrication challenges that lie beyond the 100 nanometer barrier. The problem confronting the industry is that the dominant technology used to make chips, optical lithography, used light to form patterns on silicon. Below 100 nanometers, the wavelength of light typically employed in chip production (193 nanometers and 157 nanometers) are too large to be useful. Several candidate technologies are currently vying for selection as successors to optical lithography. These include extreme ultraviolet lithography (EUV), an electron beam method called scalpel, and x-ray lithography. None has yet emerged as the preferred choice. Since it takes several years to bring the new technology up and running, the large semiconductor manufacturers are becoming increasingly concerned about the time and capital investments that will be required to keep pace with the marketplace demands.

Therefore, it would be desirable to demonstrate the feasibility of fabricating carbon nanotube molecular electronic devices with a nanosize diameter (1-50 nanometers), micro-to-submicron size length (100 -1000 nanometers), and gate few nanometers long (1-5 nanometers).

It is widely recognized that the development of molecular electronics based on carbon nanotubes would enable logic devices to be built with billions of transistors and computers that are orders of magnitude more powerful than today's machines. Smart structures in salt grain size computers, for example, could be designed with integrated logic provided by 3-D array of molecular

electronic devices. Further advances in wearable computers and other, as yet unforeseen, product possibilities will become more likely. Molecular electronics could also make possible information storage devices with immense capacity. For example, hard disks with storage capacities of terrabytes (10^{12} bytes) in small products the size of wristwatches with large storage capacities. Before these dreams become a reality, a way must be found to mass produce the molecular electronics devices. Scanning probe methods have proven feasible to fabricate single devices one atom at a time, but no way has yet been found to scale up the process. Chemically based self-assembly processes have also been suggested, but so far only the simplest structures have been built using this method. The problem of combining different materials and assembling molecular electronic devices with specific features remains a daunting challenge.

Theoretical work by Chico et. al. (L. Chico, V. H. Crespi, L. X. Benedict, S. G. Louie, and M. L. Cohen, "Pure Carbon Nanoscale Devices: Nanotube Heterojunctions," Physical Review Letters, Vol. 76, No. 6, 5 February 1996) has suggested that introducing pentagon-heptagon pair defects into otherwise hexagonal nanotube structure may create junction between two topologically or electrically different nanotubes as bases for nanoscale nanotube devices. Saito (S. Saito, "Carbon Nanotubes for Next Generation Electronic Devices," Science, Vol. 278, 3 October 1997) describes possible theoretical designs of a carbon nanotube that may function as molecular electronic devices. Those and other similar theoretical works outline the possibility to use carbon nanotubes as molecular devices but fail to propose a design of such device and a method of its fabrication.

Collins et. al. (P. Collins, H. Bando, A. Zettl, "Nanoscale Electronic Devices on Carbon Nanotubes," Fifth Foresight Conference on Molecular Nanotechnology) have experimentally demonstrated the rectification properties of single-wall carbon nanotubes. This work also fails to propose a design of carbon nanotube molecular electronic device and a method of its fabrication.

Suenaga et. al. (K. Suenaga, C. Colliex, N. Demoncy, A. Loiseau, H. Pascard, F. Willaime, "Synthesis of Nanopaticles and nanotubes with Well-Separated Layers of Boron Nitride and Carbon," Science, Vol. 278, 1997) have reported an effort to fabricate nanoscale electronic devices by fabricating concentric nanotubes out of carbon and boron nitride. This concentric design is achieved by filling-in already synthesized carbon nanotube. This design concept may work for a two-terminal device such as diode but cannot be scaled to function as a three-terminal device such as transistor. This work has also failed to explain how such device would function and has not addressed the interconnect problem.

M. Terrones et. al. (M. Terrones et. al., "Controlled production of aligned-nanotube bundles," Letters to Nature, Vol 388, July 1997) reported on efforts to fabricate horizontally aligned carbon nanotubes that may be used as electronic devices. This effort fails to describe any design of a carbon nanotube molecular device.

Most recent designs of carbon nanotube based molecular electronic devices, such as Dekker et. al. (Tans SJ, Verschueren ARM, Dekker C, "Room-temperature transistor based on a single carbon nanotube," Nature 393: (6680) 49-52, May 7, 1998), consist of a carbon nanotube spanned over two, three, or more metal electrodes. Such device may indeed function as a diode or a transistor but it cannot be scaled and cannot be connected to yet another carbon nanotube transistor.

Most recently Hu et. al. (J. Hu, M. Ouyang, P. Yang, and C. Lieber, "Controlled growth and electrical properties of heterojunctions of carbon nanotubes and silicon nanowires," Nature, Vol. 399, May 1999) has demonstrated nanoscale electronic device made of joined Si nanowire and carbon nanotube. Although successful, this nano-devices cannot be scaled up and therefore cannot be practically fabricated in a large-scale manufacturing operation.

None of the state-of-the-art research has addressed the scalability of fabricating carbon nanotube based molecular electronic devices, their interconnection, and interconnection between the molecular logic device and the outside world.

Most recently Li et. al. (J. Li, C. Papadopoulos, University of Toronto; J. Xu, Brown University, "Growing Y-junction carbon nanotubes," Nature, Vol 402, 18 Nov. 1999, pp. 253) has used nanostructured template channels to grow Y-junction carbon nanotube heterostructures from nanochannel alumina template. They first created the top pores with one voltage and then reduced it midway through the electrochemical formation of the pores. They observed that the voltage is proportional to number of pores, therefore, twice as many appeared, most branching from the original pore. This creates Y template. Catalyst was deposited electrochemically at the bottom of the template channels from which carbon nanotubes were grown. Top CNTs were close to twice the diameter of the two bottom branches. They observed that the length of the pores depends on the thickness of the substrate and the length of the Y junction depends on the timing of the current alteration. The method described in this work only addresses formation of large number of evenly distributed templates without control over pattern of the template. Use of template with variable shape to create carbon nanotube that conforms that shape and the method of producing the variable template has been disclosed in U.S. Patent No. 6,146,227, on page 5, line 43, entitled "Method for Manufacturing Carbon Nanotubes as Functional Elements of MEMS Devices" which is incorporated herein by reference. The present patent is a continuation-in-part of that issued patent.

The present invention solves all of the above problems that were not addressed by current research. The present invention identifies several designs of carbon nanotube electronic devices made of individual vertically aligned carbon nanotubes embedded in a silicon or aluminum substrate. The advantage of this design is that it is flexible and is suitable for fabrication of two-terminal (diodes) and three-terminal (transistors) carbon nanotube electronic devices, and more complex logic devices made of plurality of carbon nanotube diodes and transistors. Another advantage of the design is that

offers true 3-D architecture. Another advantage of the design is that it includes interconnects between the carbon nanotube devices and interconnects with the outside world.

The advantage of the fabrication process is that it can produce patterns of vertically grown carbon nanotubes with control over the location, dimension, and electric properties of the carbon nanotube. Another advantage of the fabrication process is that it can be scaled to produce large number of devices with a batch process. Another advantage of the fabrication process is that it can also fabricate the interconnects. Another advantage of the fabrication process is that vertical growth permits high-density packing of devices. The fabrication technology will enable device densities of 10^{12} per cm^2 (for 3 vertically stacked devices) limited only by lateral interconnect technology (among the carbon nanotubes) and the number of vertically stacked devices. With the help of lateral carbon nanotube interconnects, the technology could provide device densities to 10^{14} per cm^2. Further vertical stacking of the devices would enable magnitudes more of device densities.

The carbon nanotube devices of this invention and their fabrication process are suitable for large-scale manufacturing and interconnection of molecular electronic devices in a "salt-grain" size integrated circuit. This large-scale, low-cost approach will provide extremely fast, low-power, ultra-high-density logic and memory devices which operate at room temperature. The resulting product possibilities include fast, multi-gigaflop processors, smart structures, wearable computers, random access memories with terabyte (10^{14} bytes) capacities, and other exciting new market opportunities.

SUMMARY OF THE INVENTION

One or more of the problems outlined above may be solved by the invention of the present disclosure. The disclosure describes designs of carbon nanotube molecular devices and integrated processes for manufacturing and interconnecting a 3-D architecture of molecular devices made of carbon nanotubes, suitable for large-scale manufacturing. This large-scale, low-cost approach may provide extremely fast, low-power, ultra-high-density logic and memory devices which operate at room temperature.

In one embodiment, a logic device comprises a plurality of interconnecting carbon nanotube devices, wherein the interconnecting carbon nanotube devices comprise a plurality of electrically connected carbon nanotubes on one or differing vertical levels, and wherein the carbon nanotubes are formed within at least one nanosized catalyst retaining structure.

In another embodiment, a method of fabricating a carbon nanotube device comprises the steps of fabricating a template of nanosized catalyst retaining structures within a substrate, depositing catalyst within the nanosized catalyst retaining structures, and synthesizing carbon nanotubes that conform to the template of the nanosized catalyst retaining structures.

In another embodiment, a method for manufacturing an array of transistors comprises growing aligned carbon nanotubes within a catalyst retaining template, and introducing at least one discontinuity within a structure of the carbon nanotubes, wherein the discontinuity is a conductivity discontinuity along a vertical axis of the carbon nanotubes, wherein if one discontinuity is introduced a diode is formed and if two discontinuities is introduced a transistor is formed.

In another embodiment, a carbon nanotube transistor comprises a carbon nanotube with at least two defects therein, and wherein the defects divide the carbon nanotube into three regions with differing conductivities.

In another embodiment, a logic device comprises a substrate, a layer of insulating material in which at least one catalyst retaining structure is formed, at least one carbon nanotube formed within the catalyst retaining structure, wherein the carbon nanotube has at least two defects therein, and wherein the defects divide the carbon nanotube into at least three regions with differing conductivities.

It should be noted that many other embodiments may be apparent from this disclosure, and that such embodiments are intended to be included within the scope of the claims appended below.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings in which like reference numerals indicate like features and wherein:

FIGURE 1 shows two of many possible configurations for carbon nanotube molecular electronic devices. The structural defects (pentagon-heptagon pairs) produce a discontinuity in conductivity, believed to be the origin of the experimentally observed rectifying behavior;

FIGURE 2 shows schematic representation of a portion of a carbon nanotube molecular electronic device architecture, including vertical metallic nanotube interconnects and horizontal metallic film interconnects;

FIGURE 3 shows carbon nanotube molecular electronic device fabrication process steps;

FIGURE 4 shows the set-up for controllable electrochemical etching of the template location, diameter, shape and length;

FIGURE 5 shows the results of electrochemical etching as function of different current fluxes;

FIGURE 6 shows an example of template discontinuities possible with electrochemical etching controlled by varying the current flux as function of time;

FIGURE 7 shows an example of template discontinuities possible with electrochemical etching controlled by spacing of the templates, doping concentration, and varying the current flux as function of time;

FIGURE 8 shows method for establishing direct lateral connection between adjacent carbon nanotubes by sufficiently expanding nanotubes' diameters;

FIGURE 9 shows control of the discontinuity of the template with the help of continuous doping concentration profile of the substrate along its depth;

FIGURE 10 shows control of the discontinuity of the template with the help of discrete doping concentration profile of the substrate along its depth;

FIGURE 11 shows control of the discontinuity of the template with the help of discrete bricks of different doping concentration;

FIGURE 12 shows individual control of fabricating each template or group of templates with the help of individual electrode for each template or group or group of templates;

FIGURE 13 shows individual control of fabricating each template or group of templates with the help of masking.

DETAILED DESCRIPTION OF THE INVENTION

Preferred embodiments of the present invention are illustrated in the FIGURES, like numerals being used to refer to like and corresponding parts of the various drawings.

Figure 1 illustrates two possible configurations of carbon nanotube molecular electronic devices. The structural defects 32 -35, as illustrated in Figure 1, are pentagon-heptagon pairs which produce a discontinuity in conductivity. By fabricating vertically aligned carbon nanotube transistors with the fabrication technology disclosed in this application and related U.S. patent application Serial No. 09/669,212 entitled "Method for Manufacturing Carbon Nanotubes as Functional Elements of MEMs Devices" filed on May 11, 2000, which is incorporated herein by reference, enables device densities of 10^{12} per cm^2 limited only by lateral interconnect technology among the carbon nanotubes. Another interconnect technology may make it possible to provide device densities of 10^{14} devices per cm^2. The production of multiple carbon nanotube transistors along the vertical axis of a single carbon nanotube is also an entirely new idea.

Figure 2 illustrates complex devices in a 3-D architecture of carbon nanotube molecular electronic devices. It is possible with the innovative fabrication method to manufacture an array of electronic devices made of carbon nanotubes. The illustration shown in Figure 2 provides a stack of vertically stacked electronic devices with a first electronic device 10 and a second electronic device 12 stacked under first electronic device 10. Electronic device 10 comprises a plurality of vertically aligned carbon nanotubes 14 that are grown from a first contact plane 16. The vertically aligned

carbon nanotubes 14 are grown within vertically aligned holes within a substrate material. A contact plane 20 is provided allowing conducting interconnects 22 to contact the gates 24 of vertical carbon nanotube transistors 14. A second layer of substrate material surrounds the upper portion of the carbon nanotube transistors 14, ending in an upper contact plane 28 with bond pads 30 allowing the transistors or other logic devices within the device to be accessed from the outside world. A single carbon nanotube segment 14 will have two defects which divide the carbon nanotube 14 into three different conducting regions 36, 38 and 40 along the length of the nanotube. Altering the conductivity at many points along the nanotube axis also allows one to build multiple stacked transistors on a single carbon nanotube of the array, thus offering a 3-D architecture as illustrated by the transistor device 12 stacked beneath electronic device 10. The interconnection of carbon nanotube transistors in a given layer, or as stacked on carbon nanotube, can constitute a logic device.

The proposed carbon nanotube device fabrication process consists generally of the following process steps, which are illustrated in Figure 3: the generation of a template, such as the etched cavity 50, within a substrate material 52 or other like structure; the deposition of a catalyst 54 along the inner walls of the etched cavity 50, which is then followed by the carbon nanotube growth or synthesis of carbon nanotube 56, which is molded to conform to the etched cavity 50. Electrical contacts (interconnects) 57 may be fabricated at various places along the vertical axis of the carbon nanotube 56. It is possible to generate an array of template holes or etched cavities 50 by using an electrochemical etching on a selected substrate such as silicon or aluminum.

An example of the electrochemical setup is shown in Figure 4, wherein an array of etched templates 58 with controlled discontinuity 60 is formed within a substrate 62. It is possible, in some embodiments of the present invention, that pits 63 are pre-etched for patterning the etched templates. Depending on the desired outcome and the variation in the process parameters (primarily the etching current), the diameter of the generated template holes 50 will be between 1 nanometer and 50 nanometers. The length of the holes will equal the thickness of substrate 62. This may be on the order of one micron for a nanotube which only has a few carbon nanotube transistors along its length, to tens of microns as the 3-D nature is scaled up. For example, several carbon nanotube electronic devices are formed along the length of a nanotube by dynamically controlling the diameter of the template by controlling the current flux applied through an electrode placed on one side of the substrate. Furthermore, it will be possible to generate carbon nanotubes with different conducting properties by precisely controlling the current flux so as to produce template segments with different diameters along the vertical axis, as illustrated in Figure 5.

Figure 5 illustrates the process of forming a discontinuity in the template along its length with snap-shots at different times. It can be seen that at different times a different etch current is applied to form the template discontinuity. During the first time interval the current has been kept constant and

that produced the uniform template segment 64. At second time interval the current was increased as to produce a template segment 66. At third time interval the current was reduce to its original level and kept there. This produced the third segment 68.

Figures 6 and 7 show examples of template discontinuities possible with electrochemical etching. Preferred discontinuities comprise variations in the diameters of the templates along their lengths, producing serial segments with different diameters. An alternative way to produce discontinuities is to divide or branch the templates along their lengths, producing parallel segments with different diameters. The basic designs of CNMEDs that are possible with variable templates include diodes, transistors, and other two, three, and multi-terminal electronic devices. For any template that can be fabricated, a corresponding carbon nanotube can also be fabricated. A number of other designs can be fabricated that take advantage of the complex types of templates that are described here.

Figures 9, 10, and 11 show a method to control the discontinuity of the template by manipulating the doping concentration of the substrate and its distribution. This approach represents an effort to balance the fabrication process as to make the critical process rely on established semiconductor processes. This may lead to making the process more manufacturable and reproducible. Standard established semiconductor processes can deliver precise doses of doping over specified depths. Thin film deposition of silicon is another standard semiconductor process. When doping concentrations are controlled, the electrochemical process only needs to provide a constant current flux and the doping difference will produce the desired template shapes.

Figure 8 illustrates a method for establishing a direct lateral connection between adjacent carbon nanotubes. Such fundamentally new interconnect approaches would obviate the need for conventional lithographed metallic interconnects which limit the lateral spacing of the carbon nanotube devices. With the help of direct carbon nanotube interconnects, the technology could provide device densities to 10^{14} per cm^2. Furthermore, the ohmic contact between carbon nanotube and metal, which may be a limiting factor in the performance of the carbon nanotube devices, is replaced by nanotube-nanotube contact that is more intrinsic. Contact-less interconnection by electron tunneling or spin coupling shifts the entire paradigm of the molecular electronic device.

Figure 12 shows individual control in the fabrication of each template or group of templates with the help of individual electrodes for each template or group of templates. This approach allows different currents to be provided to different electrodes and thereby allows micro-management of the electrochemical process.

Figure 13 shows individual control of fabricating each template or group of templates with the help of masking. With this method pattern of a mask is applied to the substrate, covering an area of the substrate and exposing the rest of the substrate. An electrochemical etching can be applied to

produce a template or a group of templates with desired discontinuities, over the exposed area. This approach allows that templates with different types of discontinuities be produces at different locations on the substrate.

The present invention builds on the fabrication technology disclosed in U.S. patent application Serial No. 6,146,227 entitled "Method for Manufacturing Carbon Nanotubes as Functional Elements of MEMS Devices" which is incorporated herein by reference. The referenced patent discloses method of fabricating a nanosize catalyst retaining structure (NCRS) with precise dimensions and location that can serve as a template for a carbon nanotube with controllable orientation, diameter, location, length and shape. The carbon nanotube is synthesized by thermal deposition of hydrocarbides directly from within the template coated with catalyst. The present disclosure describes in detail the methods of changing the shape of the template and with that the shape of the synthesized carbon nanotube. The change of the carbon nanotube shape introduces controlled discontinuities in the structure of the carbon nanotube. The discontinuities in the structure of the carbon nanotube promote electronic functions that enable the design of carbon nanotube based molecular electronic devices. The present disclosure also describes designs of molecular electronic devices that can be fabricated with the template method. The present disclosure also describes methods of interconnecting the carbon nanotubes.

The present fabrication process solves the problem of introducing manufacturable controllable discontinuities along the length of a carbon nanotube. It makes sense to talk only about discontinuities along the length of the nanotube since the nanotubes are essentially one-dimensional structures with their lengths many times the sizes of their diameters. The present process claims the use of a template to shape the carbon nanotube along its length. Existing methods rely on junctions between nanotubes and on kinks in their structure to produce nanotube electronic devices.

The present fabrication process solves the problem of fabricating the nanotube devices in an integrated process instead of fabricating them separately and then assembling them. The present process involves a fabrication method that produces the carbon nanotubes in-place, embedded within the substrate. This is achieved by using templates which are embedded in the substrate and consequently producing carbon nanotubes that are also embedded in the substrate. The integrated process can also produce the interconnects among the individual carbon nanotube devices. Existing methods rely on fabricating the nanotubes separately and then placing them one-by-one on electrodes to produce nanotube electronic devices. Alternatively, they may rely on random dispersion of the nanotubes over the electrodes.

The present fabrication process solves the problem of scalable manufacturing process for production of functional carbon nanotube electronic devices. The innovative process claims fabrication method that produces an array of functional carbon nanotube electronic devices in a single

process. This is achieved by fabricating an array of templates that are precisely patterned on the substrate. In turn, the array of templates is used to produce an array of carbon nanotube devices. Existing methods rely on individually fabricated carbon nanotube devices that need to be interconnected to form a functional device. Some existing methods can also produce an array of uniformly distributed carbon nanotubes but cannot fabricate individual precisely-located nanotube or a pattern of nanotubes that are also functional.

The present fabrication process solves the problem of interconnects among the individual carbon nanotube devices and an interconnect to an external world. The present process involves fabrication of horizontal and vertical interconnects as part of the integrated fabrication process. Horizontal interconnecting is achieved by patterning metal interconnect lines in a plane sandwiched between substrate layers, combined with fabricating vertical nanotubes that pass through the metal interconnects. Alternative horizontal interconnects are achieved with the help of horizontal carbon nanotubes. Alternative horizontal interconnects are achieved by expanding the carbon nanotubes' diameters until two adjacent nanotubes touch. Vertical interconnects are achieved with the help of vertical conductive carbon nanotubes and by stacking one carbon nanotube device on top of another. Existing methods of interconnecting carbon nanotube devices rely on external contacts or on interconnects that are fabricated separately from the nanotubes. There are no existing vertical interconnect technologies.

The innovative carbon nanotube electronic device design solves the problem of existence of carbon nanotube logic devices that are molded within a substrate and not free-formed, that can be connected to other carbon nanotubes laterally or vertically, and that can form a complex 3-D architecture. This is achieved with the above mentioned innovative fabrication process. Existing carbon nanotube electronic device designs are free-formed, cannot be easily connected to other nanotubes, and are two terminal electronic devices (diodes).

The present disclosure illustrates: 1) a method of fabricating basic carbon nanotube molecular electronic devices (CNMEDs), 2) a method of fabricating complex devices in a 3-D architecture of CNMEDs, 3) basic designs of (CNMEDs) possible with the present fabrication methods, and 4) complex devices in a 3-D architecture of CNMEDs possible with the present fabrication methods.

Fabrication process

The method of fabricating the basic CNMEDs and the complex devices in a 3-D architecture of CNMEDs is a unique combination of controlled electrochemical etching and catalytic carbon nanotube growth technologies. This fabrication takes advantage of the benefits offered by the established electrochemical etching technology with the emerging technology of carbon nanotube

synthesis. The innovative fabrication process produces a 3-D pattern of carbon nanotubes synthesized by thermal deposition of hydrocarbides directly from within a 3-D template coated with catalyst.

The present fabrication process enables introducing controlled discontinuities in a template and, with that, in the structure of the carbon nanotubes. Preferably, the discontinuities will be introduced by exploiting the process of controlled electrochemical etching to vary the template diameter and shape along its length. The introduction of controlled discontinuities in the structure of the carbon nanotubes alters the bond configuration, and therefore the conductivity properties, at various points along the vertical axis of the nanotube. Figure 1 shows an example of a carbon nanotube resulting from such process.

Innovative basic CNMEDs and complex devices in a 3-D architecture of CNMEDs

This invention defines CNMEDs as electronic devices that exhibit electronic functions such as rectification, switching, and emission. CNMEDs that are possible with the innovative fabrication method include diodes, transistors, and other two, three, and multi-terminal electronic devices (such as stacked transistors and diodes). The introduction of controlled discontinuities in the structure of the carbon nanotubes enables the functionality of the CNMED devices. Introduction of integrated interconnects that connect two or more carbon nanotubes in a device able to execute a logic operation also enables the functionality of the CNMEDs. Introduction of vertical stacking of two or more carbon nanotube devices also enables the functionality of the CNMEDs. Figure 2 shows schematic representation of a portion of CNMED architecture, including vertical metallic nanotube interconnects and horizontal metallic film interconnects.

Fabrication process steps

The present carbon nanotube device fabrication process consists of the following process steps: (1) generation of template, (2) catalyst deposition, and (3) nanotube synthesis, as shown in Figure 3. Other optional steps can be added to augment the fabrication process.

Control of the carbon nanotube pattern in horizontal plane

The in-plane horizontal pattern of the templates or groups of templates can be used to control the pattern of the CNMEDs. For example, depending on the desired interconnections (i.e., depending on the particular logic gates desired), the entire process can be designed so that uniform templates (which will generate the vertical metallic interconnects) and non-uniform templates (which will generate CNMEDs) are grouped in small blocks of arrays. Metal interconnects are then used to connect the CNMEDs with the vertical metallic interconnects to create the more complex logic devices.

Control over template patterns is achieved by using means to initiate the etching at desired locations. One way of achieving this initiation is to pattern the substrate with a mask to generate pits at precise locations on a substrate that will initiate formation of a template. Another way of initiating the formation of the holes is to place an impurity, local defect, stress, or optical energy as method to initiate the formation of a template. The impurity, local defect, stress, or optical energy can be placed using masking techniques or by direct write/deposit methods. A self-organizing patterning that produces a pattern of impurity, local defect, stress, or optical energy may also be used to initiate the electrochemical etching.

Carbon nanotube interconnects

The present fabrication process includes means of interconnecting the carbon nanotube devices in horizontal and vertical planes to achieve true 3-D capable interconnection. Horizontal interconnecting can be achieved with patterned metal interconnect lines that intersect with the vertical nanotubes. Vertical interconnects can be achieved with the help of vertical conductive carbon nanotubes and by stacking one carbon nanotube device on top of another. The three dimensional architecture of CNMEDs, illustrated in Figure 2, is interconnected with a combination of horizontally patterned metal lines (using conventional lithography) and integral vertical carbon nanotube interconnects, consisting of carbon nanotubes that conduct all the way or part of the way along their vertical axes.

Horizontal interconnection is achieved by building a layered structure of doped silicon and patterned metal interconnects with interconnect pads that are strategically positioned to make sure they will interconnect with the vertically etched templates. Only the top layer of the structure is patterned to produce the horizontal pattern of the templates. Once the formation of the template is initiated, the entire template will be etched through all the layers of doped silicon and metal film. At designed locations, the vertically grown carbon nanotubes will intersect the horizontal interconnects and, in particular, the strategically positioned metal pads. The doped silicon layers also act as spacing layers with predefined vertical spacing to allow connection between the conducting, semiconducting, and nonconducting vertical segments of the carbon nanotubes. The metal lines will be used to control the functioning of the electronic devices for input, output, and addressing of the logic devices. Complex logic devices can be constructed by strategically interconnecting two or more carbon nanotubes on the same or different vertical levels.

Vertical interconnection is achieved with the help of conductive carbon nanotubes whose entire purpose is to provide vertical interconnection. These interconnect carbon nanotubes are

synthesized with the help of a cylindrical template with constant diameter. It is preferred that all templates with uniform diameter and all templates with variable diameter be synthesized on separate locations of the device away from each others so as to better control the template production. Another method of achieving vertical interconnection is to stack one carbon nanotube device on top of another from a single template.

Interconnection with the outside world may be achieved by funneling all the required internal connectors via conducting carbon nanotubes to a top level substrate where metallic bond pads are be lithographically fabricated. Bonding of gold contact pads to a carbon nanotube has already been demonstrated by Haesendonck et. al. (C. Van Haesendonck, L. Stockman, R. Vullers, Y. Bruynseraede, L. Langer, V. Bayot, E. Grivei, J. Issi, J. Heremans, C. Olk, "Nanowire bonding with the scanning tunelling microscope," Surface Science 386 (1997), 279-289). A ball grid array type of connection can then easily be achieved to connect the molecular device with the outside world.

Substrate for CNMEDs

Doped silicon is the preferred substrate material. This includes lightly and heavily doped P and N type silicon. It is preferred that the doping is introduced while the silicon crystal is grown in order to produce uniform concentration of doping along the thickness of the substrate. For thin silicon layers, the doping can be introduced by ion implantation.

Alternatively, aluminum is the next preferred substrate. The purity of the starting aluminum is important factor for electrochemical etching of templates. Other substrate choices include materials or composites that are suitable for electrochemical etching. A gallium arsenide substrate is also acceptable as substrate for electrochemical etching of templates.

To achieve the 3-D architecture described above, the substrate has to be prefabricated to include the metal interconnects. A prefabricated substrate includes a layered structure of doped silicon and patterned metal interconnects. Masking oxide or nitride layers will be used to produce the patterned metal lines. The most common interconnect materials include metals such as aluminum, copper, tungsten, titanium, nickel, chromium and various metal alloys. The silicon layer may be epitaxially grown, or it may be deposited. Any silicon, including amorphous, polysilicon, or crystalline silicon is acceptable as a substrate for electrochemical etching of templates. It is preferred that the substrate be made of crystalline silicon. Acceptable ways of producing the crystalline silicon include depositing polysilicon over the metal layer, implanting it with the right dose of dopants, and recrystallizing it over in a high temperature baking process. Alternatively, the desired substrate can be bonded together.

A prefabricated aluminum substrate would include layers of aluminum and patterned metal interconnects. The desired substrate can be fabricated by subsequent stacking of deposited metal lines and deposited aluminum that may have to be recrystallized.

Electrochemical etching process

The preferred embodiment of the present device fabrication process relies on electochemical and photoelectrochemical etching as a mechanism of generating the template. The methods of controlling an electrochemical etching process of N-type silicon are described in detail by Lehmann et. al. (V. Lehmann and H. Foll, "Formation Mechanism and Properties of Electrochemically Etched Trenches in n-Type Silicon," J. Electrochem. Soc., Vol. 137, No. 2, February 1990) which is incorporated herein by reference. The teachings of Lehmann also apply to P-type silicon, with minor adjustments known to those skilled in the art. Other research (G. Bomchil, A. Halimaoui, I. Sagnes, P. Badoz, I. Berbezier, P. Perret, B. Lambert, G. Vincent, L. Garchery, J. Regolini, "Porous silicon: material properties, visible photo- and electroluminecsence," Applied Surface Science 65/66, 1993, pp. 394-407; H. Ohji, S. Lahteenmaki, P. French, "Macro porous silicon formation for micromachining," Proc. SPIE-Int. Soc. Opt. Eng., 3223, 1997, pp. 189-197) describes porous silicon formation and its use with patterning for micromachining.

An example of electrochemical set-up of this invention is shown in Figure 4. In one such example of electrochemical etching P++, P+, N-, and N-- doped silicon can be etched with a diluted HF acid (25% HF, 25% de-ionized water, 50% ethanol) and current densities of 10 mA/ cm^2.

Electrochemical etching of a layered substrate of silicon and metal film is slightly different from electrochemical etching of single layer of silicon. After the template reaches the depth where the metal layer exists, the etchant will simply dissolve the thin metal layer and will continue with the etching of the silicon. This process can be used to monitor the current load and to determine when the etching of the silicon has reached the metal layer. This information may be used for control purposes. After the metal has been dissolved, there will still be a ring of metal on the circumference of the template.

After the template has been fabricated, one can optionally bake the sample in oxygen environment as to oxidize the walls of the template and electrically isolate the template walls from the surrounding substrate. This process will disable or reduce any current leakage from one nanotube (that will be synthesized within the template) to an adjacent one. This oxidation process will also shrink the diameter of the template as oxygen atoms bond to silicon atoms. Alternatively, the template walls can be baked in nitrogen atmosphere to create a nitride wall. Any other reduction of the surface with another gas may also be implemented to achieve similar goals.

Control of the carbon nanotube discontinuities

The discontinuities of the template along the vertical axis of the template are used to control the bond configuration, and therefore the conductivity properties, at various points along the vertical axis of the nanotube. Preferably, the discontinuities will be introduced by exploiting the process of controlled electrochemical etching to vary the template holes along their lengths. The preferred means for achieving discontinuities is to vary the diameters of the templates along their lengths, producing serial segments with different diameters. An alternative way to produce discontinuities is to divide or branch the templates along their lengths, producing parallel segments with different diameters.

Control of the electrochemical etching process is the most critical step in the preferred embodiment of the present fabrication process. Variation of the process parameters, such as the current density, the concentration of the etchant, the doping of the silicon substrate, the luminescence, the crystal orientation of the substrate, and the adjacent template spacing can be used to control the template discontinuities and to thereby generate carbon nanotubes with different conducting properties.

Dynamic control of the diameters of the templates along their depth is achieved by controlling the process parameters as a direct function of the depth of penetration of the etchant, and an indirect function of the etching rate and the etching time. In the preferred embodiment, the current flux is precisely controlled as function of time so as to produce template segments with different diameters along the vertical axis (Figure 5). In one example, the electrochemical etching takes 10 minutes, where during the first 4 minutes, the current density is held at constant 3 mA/cm^2, followed by 2 minute etching at 10 mA/cm^2, followed by 4 minute etching at 3 mA/cm^2. It is assumed that the doping concentration is constant over the thickness of the substrate. The resulting template will be a cylindrical template with a bulge in the middle (Figure 6A). If the order of the current density is switched, the resulting template will be an hour-glass shaped template (Figure 6B). Examples of other possible discontinuities resulting from variations in the current flux as function of time are shown in Figures 6C-E. In Figure 6C, the process of Figure 6A is repeated two times. In Figure 6D, the current density has been increased, but it has not been decreased. In Figure 6E, the current density is increased with a constant rate to produce template with tapered walls. Any other combination of the above examples is also possible with the present process.

In another embodiment, the adjacent template spacing, which is produced by patterning the initiation location and spacing of the template, can be used as a controlling parameter in conjunction with the doping concentration of the substrate. If the template spacing is too far in relation to the doping density, the templates will divide, as illustrated in Figure 7A, or branch, as shown in Figure 7B. If the reverse is true, the template will join. Precisely controlling the current flux as function of

time (indirectly as function of the depth of penetration) can produce a template that divides or branches in a desirable fashion along the vertical axis, effectively producing parallel template segments with different diameters. Figure 7C illustrates more complex templates that can be produced with this process. Any other combination of the above examples is also possible with the present process.

The methods to control the discontinuity of the template and therefore the discontinuity of the carbon nanotube are also applicable to an aluminum substrate. The current density, the concentration of the etchant, and the adjacent template spacing are suitable process parameters that can be used to control the template discontinuities and thereby generate carbon nanotubes with different conducting properties. Substrate doping, luminescence, and the crystal orientation are not applicable process parameters in etching an aluminum substrate.

Many different templates can be fabricated with the electrochemical etching technology described above for use as templates to fabricate carbon nanotubes. These variations are contemplated to be within the skill of a person of ordinary skill in the art and are therefore believed to be within the scope of this disclosure and the appended claims.

Control of the carbon nanotube diameter and length

Process parameters, such as the current density, the concentration of the etchant, the doping of the silicon substrate, the luminescence, the crystal orientation of the substrate, and the adjacent template spacing all influence the diameter of the initiated template. Depending on the size of the desired electronic device, it is preferred that the diameter of generated template holes be between 1 and 50 nm. The electrochemical etching is also capable of generating templates that are up to microns in size. The length of the holes can be controlled by timing the entire process and may equal the thickness of the substrate. This may be on the order of one micron for a nanotube which has only one or few CNTs along its length, to tens of microns as the 3-D nature is scaled up (i.e., tens of CNTs along the length of a nanotube).

Catalyst deposition in the templates

The catalyst deposited within an etched cavity or template shape may be a metal catalyst, such as iron, nickel, copper, or other like catalysts known to those skilled in the art,

After the template is formed, it is coated with a metal catalyst (Fe, Ni, Co, etc.). This can be achieved by chemical deposition (G. Che, B. Lakshimi, C. Martin, E. Fisher, "Chemical Vapor Deposition Based Synthesis of Carbon Nanotubes and Nanofibers Using a Template Method," Chem. Mater., 10, '98) or electrodeposition (A. Bard, L. Faulkner, Electrochemical Methods: Fundamentals and Applications, John Willey & Sons, 1980, p. 372). Such techniques have already been

demonstrated. For the case of electo-oxidation and electro-deposition, we may utilize the same electrical contacts as those used for the electrochemical etching. The main challenge in this step is the uniform deposition or formation of catalysts within the template. It is desirable that the template be kept wet before proceeding with the catalyst deposition, as drying of the template walls creates surface tension that makes the catalyst diffusion more difficult. For templates with more complex shape, the diffusion of the catalyst molecules within the network of templates will be slower. A DOE can be conducted to determine the timing required to diffuse the catalyst penetration. Mechanical vibration, vacuum suction, temperature, and use of surfactants may be employed to improve the diffusion process.

Alternatively, the deposition of the metal catalyst can be done concurrently with the electrochemical etching by incorporating traces of the metal catalyst in the etch solution. For example, iron salt may be added to the HF concentration mentioned above to introduce the catalytic metal into the etch solution. As the electrochemical etching proceeds, the metal catalyst will concurrently be deposited on the walls of the template. One advantage of this method of catalyst deposition is that it is not affected by the complexity of the template network since it is distributed concurrently with the etchant. This is the preferred method of catalyst deposition within the template.

Carbon nanotube synthesis

Due to the location of the catalyst, carbon nanotubes grow and are encased by the walls of the hole, causing carbon nanotubes to grow radially inwards. The diameter of the nanotube is also confined by the inner walls of the hole. Thermal deposition of hydrocarbides or CVD processes can be used to grow carbon nanotubes within the templates. In this process, a nanotube's thickness is controlled by timing the CVD process and terminating it as needed. A carefully designed process may lead to a synthesis of single wall carbon nanotubes. Alternatively, multi-walled carbon nanotubes may also be generated.

The challenge here is to achieve adequate quality of the generated carbon nanotubes, namely their conductivity profile and purity of the carbon nanotube bond. The generated carbon nanotubes will take the shape of the templates where they are synthesized. A template with variable diameters along its length will produce carbon nanotubes with variable diameters along their lengths. A template with divided or branched legs will produce carbon nanotubes with divided or branched legs. The appropriate change in the diameter of the carbon nanotube induces the desired change in the conductive properties of the carbon nanotube. For example, slightly constricting a metallic nanotube induces a pentagon-heptagon defect, resulting in a semiconducting segment of a nanotube (Figure 1). The use of a template to mold and bound the shape of the carbon nanotube is unique.

After the carbon nanotube is synthesized in a layered structure of silicon and metal, the nanotube will make contact with the metal ring which is left after etching away the template through the metal film, thereby establishing metal contact. Thermal heating or electrical load may have to be applied to diffuse the metal layer with the carbon nanotube and to establish good electrical contact.

Carbon nanotube molecular electronic devices

The basic designs of CNMEDs that are possible with the innovative fabrication method include diodes, transistors, and other two, three, and multi-terminal electronic devices (such as stacked transistors and diodes). A number of other designs can be fabricated that take advantage of the complex types of templates that are described above. For any template that can be fabricated, a corresponding carbon nanotube can also be fabricated.

To create a logic device, one or two pentagon-heptagon defects, generated by slightly constricting a metallic nanotube, connected back-to-back and biased properly with external connections, will function as diode or transistor, respectively. The nanotube metallic segments with uniform diameter constitute vertical connectors, and can be connected to the carbon nanotube device by patterned metal lines (Figure 2).

A single carbon nanotube segment with one discontinuity, producing two different conducting regions along the nanotube, will constitute a carbon nanotube diode in one embodiment. The carbon nanotube diode is embedded into a substrate and includes integrated source and drain electrodes. The carbon nanotube diode may be grown vertically aligned.

The carbon nanotube transistor of one embodiment is a single carbon nanotube segment with two discontinuities, producing three different conducting regions along the nanotube. The carbon nanotube transistor of this embodiment is embedded into a substrate and includes integrated source, drain, and gate electrodes. The transistor may also be grown vertically aligned.

Altering the conductivity at many points along the nanotube axis will also allow us to build multiple stacked transistors from each single carbon nanotube of the array, thus offering a true 3-D architecture. Therefore, a carbon nanotube transistor of another embodiment constitutes two or more carbon nanotube transistors, each with two discontinuities, stacked vertically. The stacked transistor of this invention is embedded into a substrate and includes integrated source, drain, and gate electrodes for each transistor.

A generic logic device of this invention is constructed by the interconnection of a few (typically three) devices in a given layer, or a few stacked devices on a single carbon nanotube. This generic logic device has 3-D architecture.

Advantages provided by various embodiments of the present invention may include flexibility and reproducibility of synthesizing carbon nanotubes which have dimensions and shapes determined

by a vertically aligned template, wherein these carbon nanotubes exhibit rectifying behavior. By reproducing a plurality of these carbon nanotubes, it is possible to show the scalability by fabricating hundreds of carbon nanotube devices with similar, if not identical, electrical characteristics. These electrical characteristics may be verified by testing the rectifying behavior of a carbon nanotube device with the help of scanning probe tools by testing two or three points along the carbon nanotube device. The comparison of the results among multiple carbon nanotube devices fabricated within the same processes demonstrates similar, if not identical, electrical characteristics. Thus, a controllable electrochemical process that allows the fabrication of templates with desired dimensions is described. From this template with desired dimensions, carbon nanotube devices may be fabricated with variable diameters along a vertical axis. By synthesizing or fabricating the carbon nanotube molded by the template with a reliable and reproducible process, it is possible to, with a high degree of quality, synthesize crystalline carbon nanotube with reproducible electrical characteristics. These carbon nanotube devices may be interconnected to create and utilize carbon nanotube transistors and other similar devices. These interconnects may comprise carbon nanotube-to-carbon nanotube, or carbon nanotube-to-metal, or carbon nanotube-to-another-like-conducting-material. The electrical or chemical etching processes may be manipulated so as to produce templates with distributed and desired density patterns of carbon nanotube devices which, when interconnected, may comprise a full working logic device.

The electrical properties of carbon nanotubes comprise, among other things, the particularly high conductivity and rectification properties discussed above. It is desirable to fabricate carbon nanotube transistors in an organized manner and interconnect these carbon nanotube transistors with conducting interconnects. It is extremely desirable to have a process designed to fabricate carbon nanotube molecular electronic devices with both scalability and manufacturability.

Part of the uniqueness of the present approach is that carbon nanotube transistor fabrication can be scaled to a large number of devices with the same batch processes. The large scale, low cost approach of the present disclosure provides extremely fast, low power, ultra-high density logic and memory devices which operate at room temperature. There are at least two generations of device architecture that can be based on the approach of this disclosure. The first generation would use a combination of horizontally patterned metal films, fabricated using conventional lithography and integrated vertical structures consisting of carbon nanotubes. A second generation architecture would be based on etching horizontal holes to provide horizontal interconnection with the help of a horizontal conductive-only carbon nanotube instead of metallic lines.

Additional Embodiments

In another embodiment of the present invention, horizontally etched templates may be employed to generate horizontal interconnection with the help of horizontal conductive-only carbon nanotubes instead of metallic interconnects. This task can be accomplished with the help of side electrodes, either on the surface or buried in the layer of silicon and metal film. For example, two electrodes located on a same level that are energized locally may produce a horizontal template. One needs to ensure that etchant can access the silicon that needs to be dissolved. Horizontal carbon nanotube interconnects may also be used as part of the carbon nanotube electronic device and not only as interconnects.

Alternatively, it is possible to establish direct lateral connections between the nanotubes by sufficiently expanding a conducting nanotube's diameter as to allow them to touch or tunnel electrons, as shown in Figure 8. The electron tunneling connection may also be the basis for a quantum interacting between the nanotubes beyond the interconnect function it provides. Such fundamentally new interconnect approaches would obviate the need for conventional lithographed metallic interconnects or horizontal carbon nanotube interconnects and provide contact-less interconnection. This approach would also enable greatly increased device density.

In another embodiment of the present invention, the desired discontinuity of the template may be achieved by altering the doping concentration profile of the substrate along its depth. The doping profile may be continuous or discontinuous. For example, continuous profile may be produced with the help of ion implantation or thermal diffusion that may achieve the desired dopant profile. Figure 9 illustrates a dopant profile that was achieved with double sided dopant implantation. A discontinuous profile may be achieved by producing a layered structure of substrates with different doping concentrations as shown in Figure 10. Application of continuous current density to both samples during an electrochemical etching will produce template with variable diameter along its length. Those templates will in turn produce variable shaped carbon nanotubes as illustrated in Figures 9 and 10.

In another embodiment of the present invention, a brick-like structure of substrate, where each brick has desired doping concentration, may be used to fabricate multiple templates, each with its own template profile. The discontinuity produced by each brick depends on the level of its doping. Figure 11 illustrates the design of this brick-like structure. Application of continuous current density to such sample during an electrochemical etching will produce a template with a profile that depends on which brick it passes through. The brick-like structure may be constructed with the help of multi-layer patterning, masking, and dopant implantation.

One alternative to using a platinum mash electrode is to pattern platinum electrodes on the substrate and provide the required current flux on a localized area of the substrate. Platinum is

resistant to the HF but other material may be used as electrode especially if it is buried in a layer of silicon. This invention allows that we provide different current to different electrodes and therefore micro-manage the electrochemical process. In this embodiment, individual control of fabricating each template or group of templates may be achieved by producing an individual electrode for each template or group of templates. The electrode will carry the desired current recipe for that template or group of templates. For example, in one area of the sample, we may etch with constant current (Figure 12A,) and in the adjacent area, we may vary the current to produce variable template (Figure 12B). In another example, we may use two electrodes that are laterally off from each other and are vertically separated by a silicon substrate to produce sloped templates with respect to the horizontal substrate, as illustrated in Figure 12C. Alternatively, optical illumination with a pattern matching the pattern of the templates may be used in lieu of the individual electrodes to control the shape of each template or group of templates. The optical pattern may be generated by a lithographic tool.

In another embodiment of the present invention individual control of fabricating each template or group of templates can be achieved with the help of masking (Figure 13). Masking is therefore used to micro-manage the electrochemical process. With this method selected areas of the substrate will be masked while other will be exposed. Using this method an individual template or group of templates with desired discontinuities can be fabricated from the exposed areas while the masked areas will remain unprocessed (Figure 13A). In subsequent process steps the pattern of the mask can be changed so that other areas of the substrate can now be processed. Therefore, another individual template or group of templates can be fabricated from the exposed areas with discontinuities different from the first set of fabricated templates (Figure 13B). The advantage of this approach is that allows selective processing of the substrate, where each area is processed with its own recipe of desired discontinuities. The masking layer needs to be resistant to the etchant.

In another embodiment, the material for one or more of the horizontal interconnects may also be a catalyst material. This process allows the metal catalyst to already be present when the template uncovers the layer. In some applications, this may be the most suitable way to provide the catalyst.

Although the present invention has been described in detail, it should be understood that various changes, substitutions and alterations can be made hereto without departing from the spirit and scope of the invention as described by the appended claims.

CLAIMS

1. A logic device, comprising:

a plurality of interconnecting carbon nanotube devices, wherein said interconnecting carbon nanotube devices comprise a plurality of electrically connected carbon nanotubes on one or more levels of a substrate, and wherein said carbon nanotubes are formed within at least one nanosized catalyst retaining structure in said substrate.

2. The logic device of Claim 1, further comprising one or more electrical bond pads coupled to the plurality of carbon nanotube devices and configured to provide external electrical connections to the logic device.

3. The logic device of Claim 1, wherein said plurality of interconnecting carbon nanotube devices is electrically connected via patterned electrically conducting films.

4. The logic device of Claim 1, wherein said plurality of interconnecting carbon nanotube devices is electrically connected via patterned electrically conducting carbon nanotubes.

5. The logic device of Claim 1, wherein said plurality of interconnecting carbon nanotube devices are electrically connected via a combination of patterned electrically conducting films and patterned electrically conducting carbon nanotubes.

6. The logic device of Claim 3, wherein said patterned electrically conducting films are metallic films.

7. The logic device of Claim 1, wherein a plurality of carbon nanotube devices are formed on a single carbon nanotube and wherein said plurality of carbon nanotube devices are electrically isolated by non-conducting segments of said single carbon nanotube.

8. The logic device of Claim 2, wherein said electrical bond pads comprise metallic bond pads.

9. The logic device of Claim 8, wherein said metallic bond pads are lithographically fabricated.

10. The logic device of Claim 1, wherein said device is fabricated on a doped silicon substrate.

11. The logic device of Claim 1, wherein said device is fabricated on an aluminum substrate.

12. The logic device of Claim 1, wherein said device is fabricated on a substrate suitable for electrochemical etching.

13. The logic device of Claim 12, wherein said substrate further comprises metal interconnects coupled to said carbon nanotube devices.

14. The logic device of Claim 12, wherein said substrate comprises layers of doped crystalline silicon and patterned metal interconnects.

15. The logic device of Claim 12, wherein said substrate is fabricated by stacking of deposited metal lines and epitaxialy grown or deposited silicon layer, followed by ion implantation and recrystallization of the silicon.

16. The logic device of Claim 12, wherein said substrate further comprises a plurality of layers bonded together.

17. The logic device of Claim 11, wherein said substrate further comprises layers of aluminum and patterned metal interconnects fabricated by stacking deposited metal lines and recrystallized deposited aluminum.

18. A method of fabricating a carbon nanotube device, comprising the steps of:
fabricating a template of nanosized catalyst retaining structures within a substrate;
depositing catalyst within said nanosized catalyst retaining structures; and
synthesizing carbon nanotubes that conform to said template of said nanosized catalyst retaining structures.

19. The method of Claim 18, wherein said template bounds a pattern of said carbon nanotube devices.

20. The method of Claim 18, wherein said template bounds a length of said carbon nanotube devices.

21. The method of Claim 18, wherein said template bounds a vertical profile of said carbon nanotube devices.

22. The method of Claim 18, wherein said nanosized catalyst retaining structures comprise uniform holes used to synthesize vertical carbon nanotube interconnects and non-uniform holes used to synthesize carbon nanotube devices.

23. The method of Claim 18, further comprising the step of interconnecting carbon nanotube devices with electrically conducting interconnects to form logic devices.

24. The method of Claim 18, wherein said template is fabricated by etching said substrate at specified locations.

25. The method of Claim 24, wherein said specified locations are patterned using lithographic techniques.

26. The method of Claim 18, wherein fabricating said template comprises placing of an impurity, local defect, stress, or optical energy to initiate formation of said nanosized catalyst retaining structures.

27. The method of Claim 22, wherein said non-uniform holes have discontinuities in diameter along a vertical axis of said holes.

28. The method of Claim 27, wherein said template is generated by using electrochemical etching or photo-electrochemical etching.

29. The method of Claim 28, wherein said electrochemical etching process is varied by process parameters selected from the group consisting of current density, concentration of the etchant, doping of the silicon substrate, and luminescence.

30. The method of Claim 29, wherein dynamic control of a diameter of a hole of said templates along a vertical axis is achieved by controlling said process parameters as a function of depth of penetration, etching rate and etching time.

31. The method of Claim 29, wherein dynamic control of a diameter of a hole of said templates along a vertical axis is achieved by controlling a current flux as a function of time.

32. The method of Claim 29, wherein said electrochemical etching of a doped silicon substrate is achieved with a diluted HF acid and current densities of 10 mA/ cm^2.

33. The method of Claim 32, wherein said electrochemical etching is configured to produce a cylindrical template with a bulge or an hour-glass shaped template.

34. The method of Claim 32, wherein said electrochemical etching is configured to produce a cylindrical template with a diameter between 1 and 50 nm.

35. The method of Claim 28, wherein said substrate is an aluminum substrate, and wherein said electrochemical etching process is varied by process parameters selected from the group consisting of current density and concentration of the etchant.

36. The method of Claim 35, wherein dynamic control of a diameter of a hole of said templates along a vertical axis is achieved by controlling said process parameters as a function of depth of penetration, etching rate and etching time.

37. The method of Claim 35, wherein dynamic control of a diameter of a hole of said templates along a vertical axis is achieved by controlling a current flux as a function of time.

38. The method of Claim 35, wherein said electrochemical etching of a doped silicon substrate is achieved with a diluted HF acid and current densities of 10 mA/ cm^2.

39. The method of Claim 35, wherein said electrochemical etching is configured to produce a cylindrical template with a bulge or an hour-glass shaped template.

40. The method of Claim 35, wherein said electrochemical etching is configured to produce a cylindrical template with a diameter between 1 and 50 nm.

41. The method of Claim 18, wherein catalyst comprises a metal catalyst.

42. The method of Claim 41, wherein said metal catalyst is selected from the group consisting of Fe, Ni, and Co.

43. The method of Claim 41, wherein said catalyst is deposited using chemical deposition or electro-deposition.

44. The method of Claim 41, wherein said deposition of said metal catalyst is achieved concurrently with said fabrication of said template by incorporating a metal catalyst in an electrochemical etching solution.

45. The method of Claim 44, wherein said etching solution comprises HF with traces of iron to introduce catalytic metal into said etching solution.

46. The method of Claim 18, wherein synthesizing said nanotubes comprises thermal deposition of hydrocarbides using a CVD process.

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47. A method for manufacturing an array of transistors, comprising:

growing aligned carbon nanotubes within a catalyst retaining template; and

introducing one or more discontinuities within a structure of said carbon nanotubes, wherein said discontinuities are conductivity discontinuities along a vertical axis of said carbon nanotubes, wherein if one discontinuity is introduced a diode is formed and if two discontinuities is introduced a transistor is formed.

48. The method of Claim 47, wherein said discontinuities comprise variations in a diameter of said carbon nanotubes or impurities in said carbon nanotube.

49. The method of Claim 48, wherein said variations in said diameter of said carbon nanotubes are achieved by varying an electrochemical etch process.

50. The method of Claim 47, wherein said catalyst retaining structure is formed on a substrate.

51. The method of Claim 47, wherein said at least two discontinuities comprise pentagon-heptagon pairs.

52. The method of Claim 47, wherein more than at least two discontinuities are introduced within said structure of said carbon nanotube to produce one or more carbon nanotube transistors along said vertical axis.

53. A carbon nanotube transistor, comprising:

a carbon nanotube with at least two defects in said carbon nanotube, and wherein said defects divide said carbon nanotube into three regions with differing conductivities.

54. The carbon nanotube transistor of Claim 53, wherein said defects comprise variations in a diameter of said carbon nanotubes.

55. The carbon nanotube transistor of Claim 54, wherein said variations in said diameter of said carbon nanotubes are achieved by varying an electrochemical etch process.

56. The carbon nanotube transistor of Claim 53, wherein said catalyst retaining structure is formed within a substrate.

57. The carbon nanotube transistor of Claim 53, wherein said at least two discontinuities comprise pentagon-heptagon pairs.

58. The carbon nanotube transistor of Claim 53, wherein more than two discontinuities are introduced within said structure of said carbon nanotube to produce a plurality of carbon nanotube transistors along said vertical axis.

59. A logic device, comprising:

a substrate;

a layer of insulating material in which at least one catalyst retaining structure is formed;

at least one carbon nanotube formed within said catalyst retaining structure, wherein said at least one carbon nanotube has at least two defects in said carbon nanotube, and wherein said defects divide said carbon nanotube into at least three regions with differing conductivities.

60. The logic device of Claim 59, wherein said defects comprise variations in a diameter of said carbon nanotubes;

61. The logic device of Claim 60, wherein said variations in said diameter of said carbon nanotubes are achieved by varying an electrochemical etch process.

62. The logic device of Claim 59, wherein said catalyst retaining structure is formed on a substrate.

63. The logic device of Claim 59, wherein said at least two discontinuities comprise pentagon-heptagon pairs.

64. The logic device of Claim 59, wherein more than two discontinuities are introduced within said structure of said carbon nanotubes to produce a plurality of carbon nanotube transistors along said vertical axis.

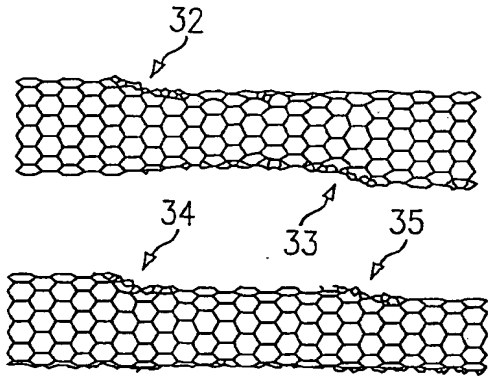

FIG. 1

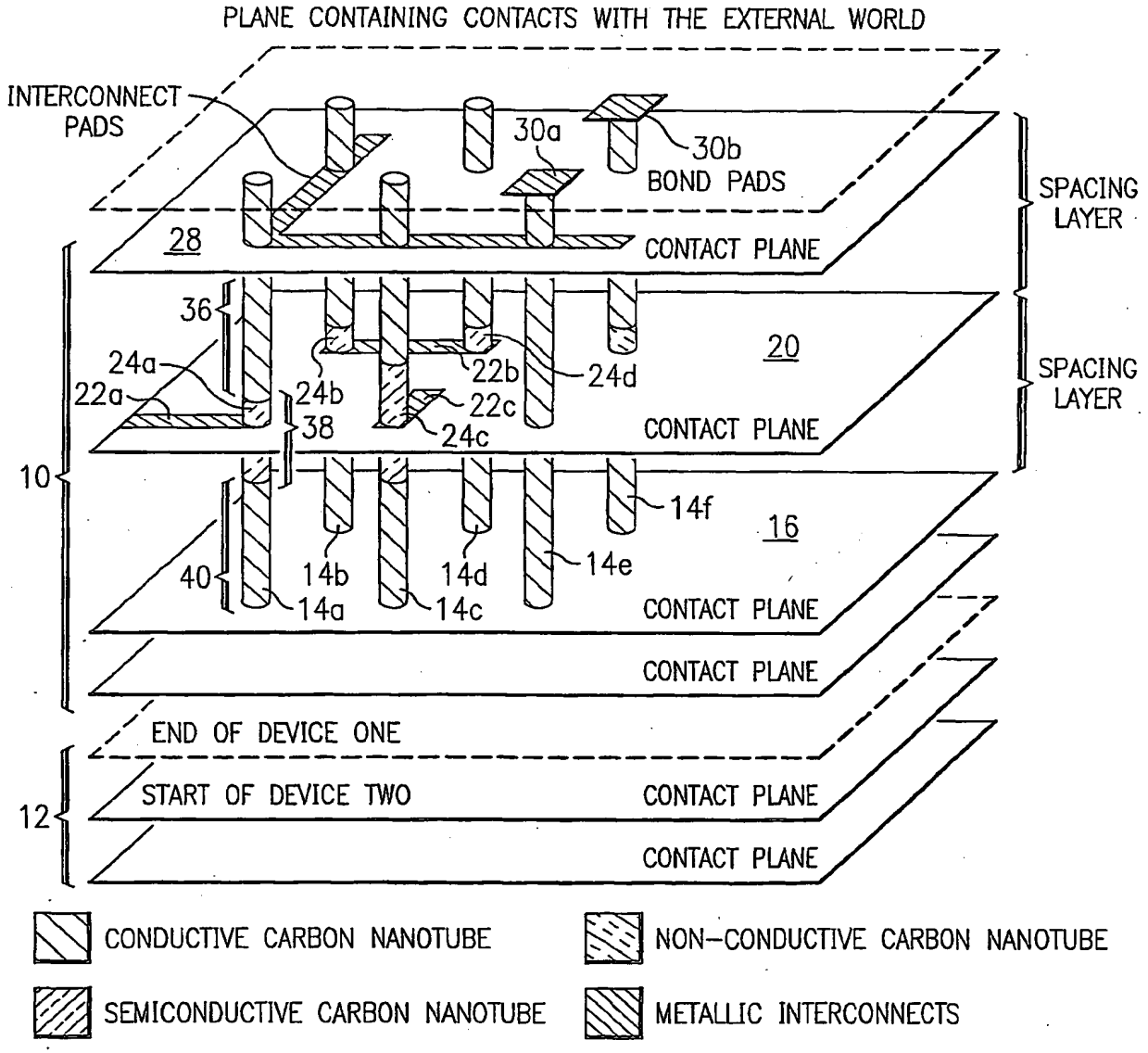

FIG. 2

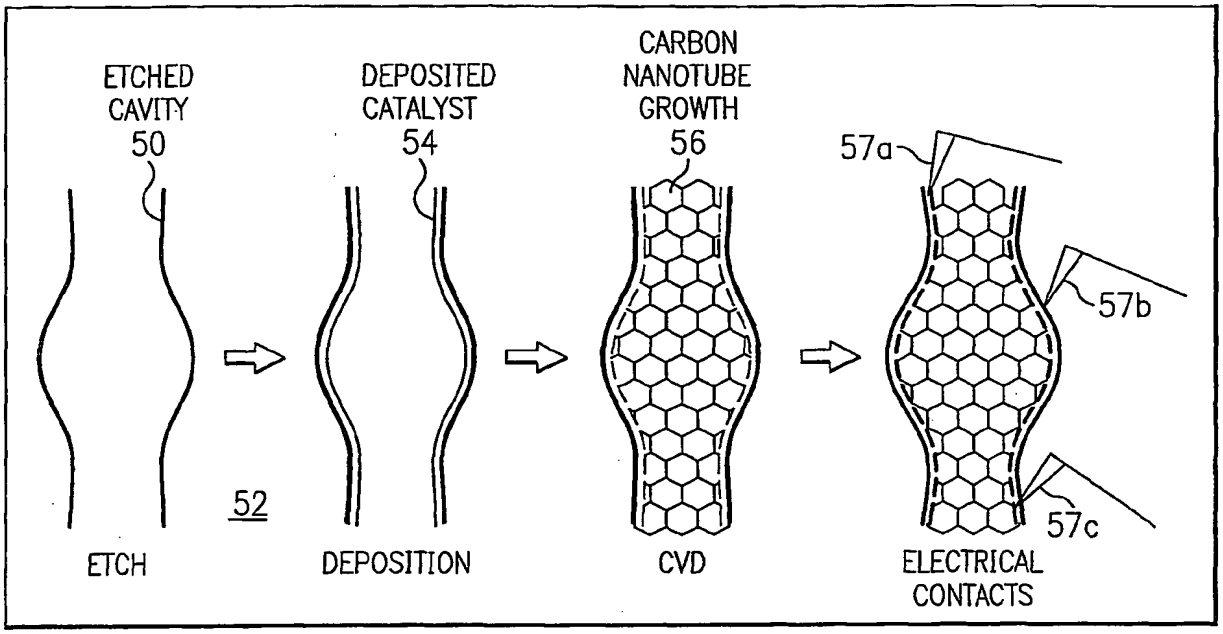

FIG. 3

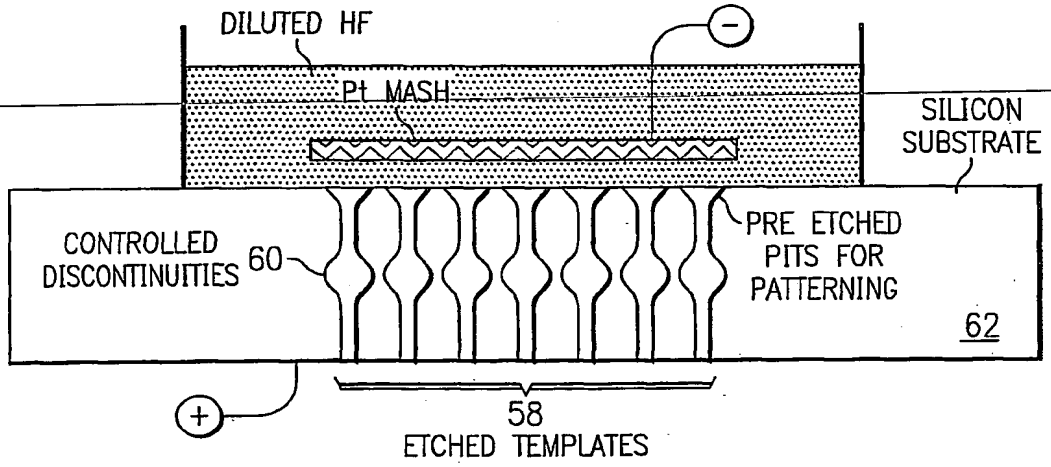

FIG. 4

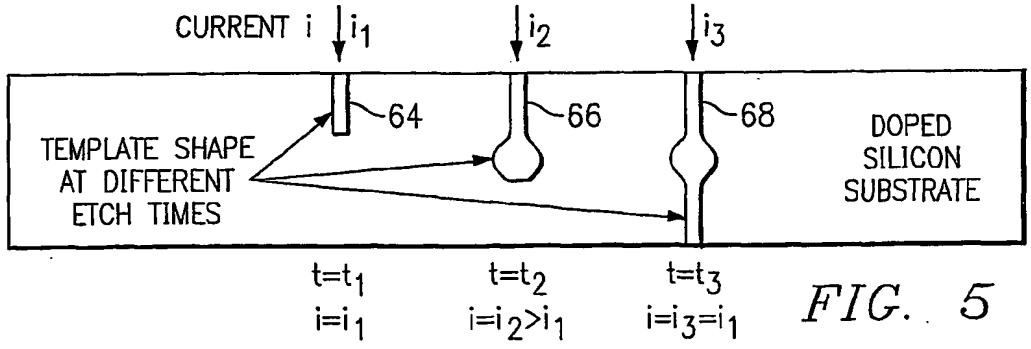

FIG. 5

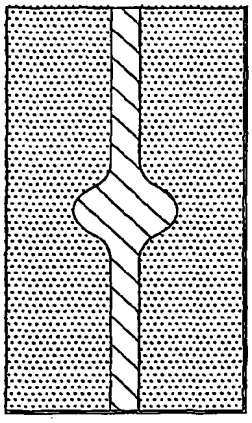

FIG. 6A

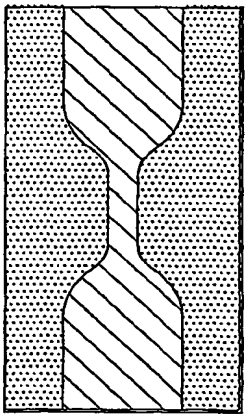

FIG. 6B

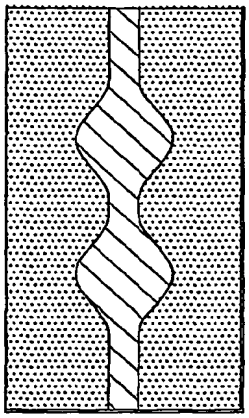

FIG. 6C

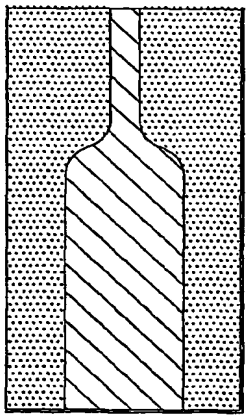

FIG. 6D

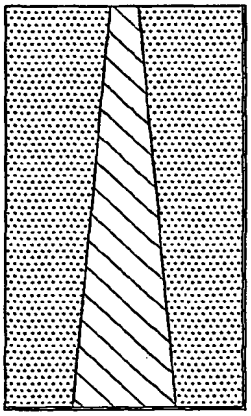

FIG. 6E

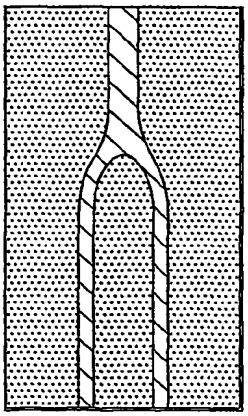

FIG. 7A

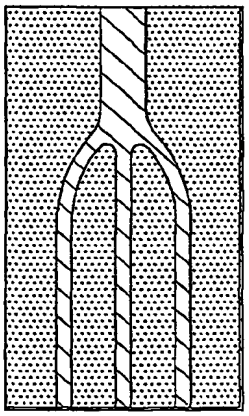

FIG. 7B

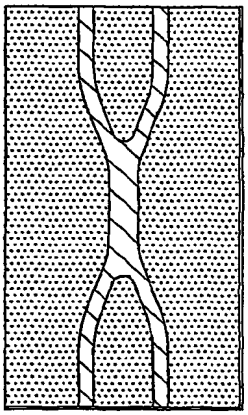

FIG. 7C

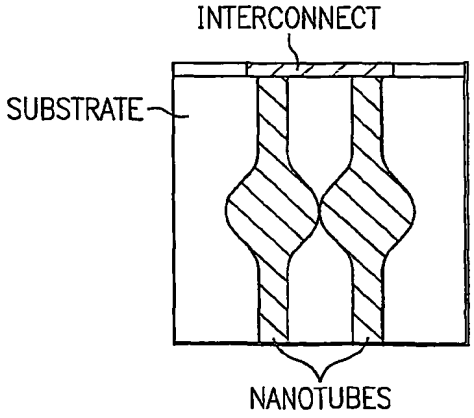

FIG. 8

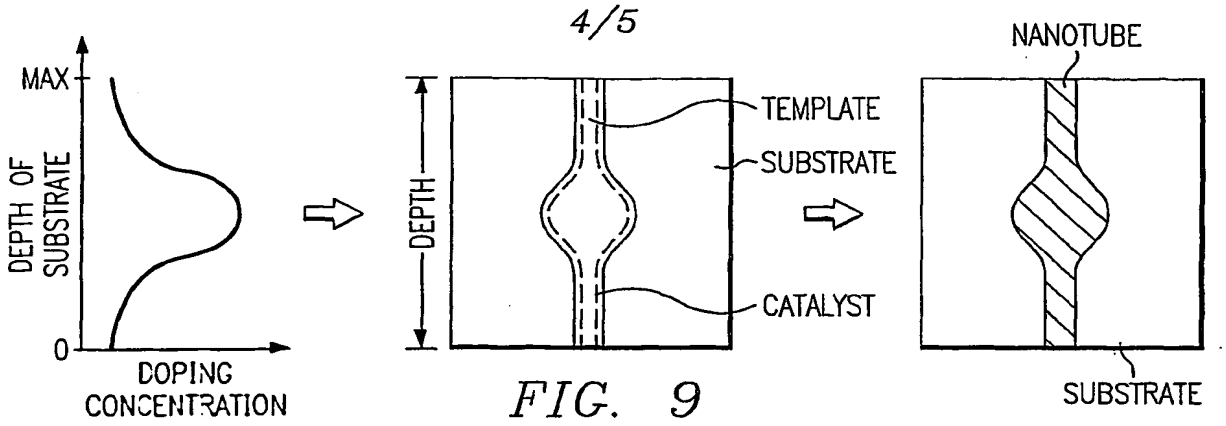

FIG. 9

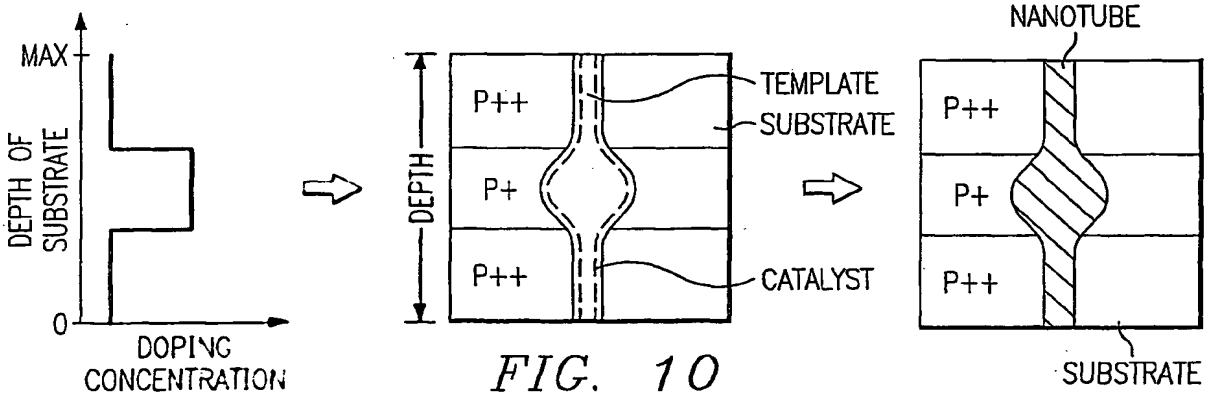

FIG. 10

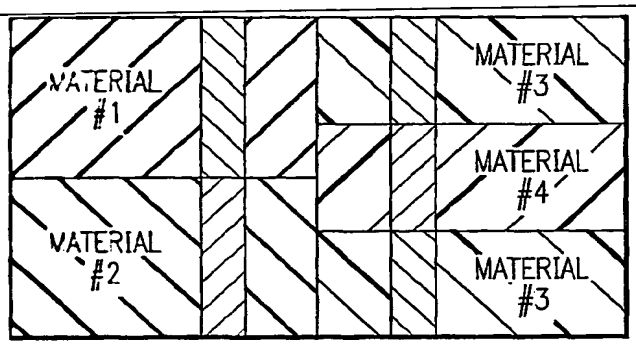

FIG. 11

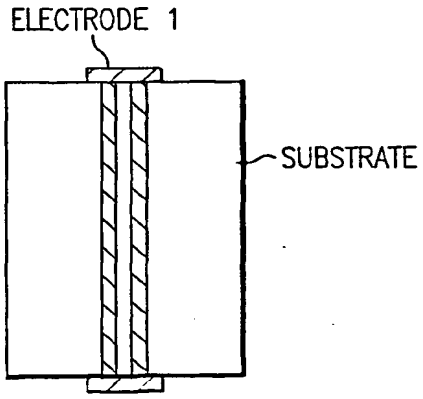

FIG. 12A

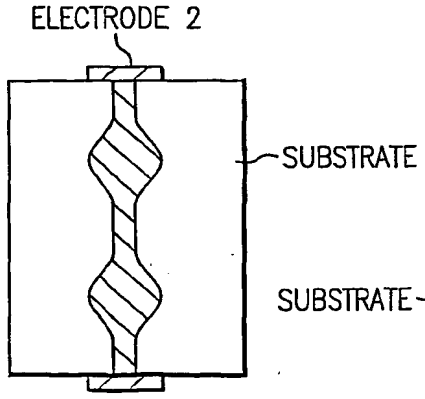

FIG. 12B

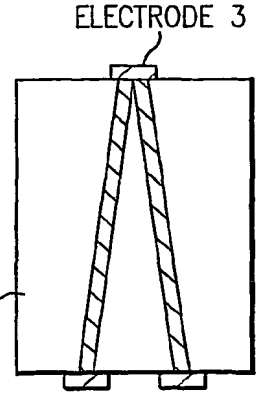

FIG. 12C

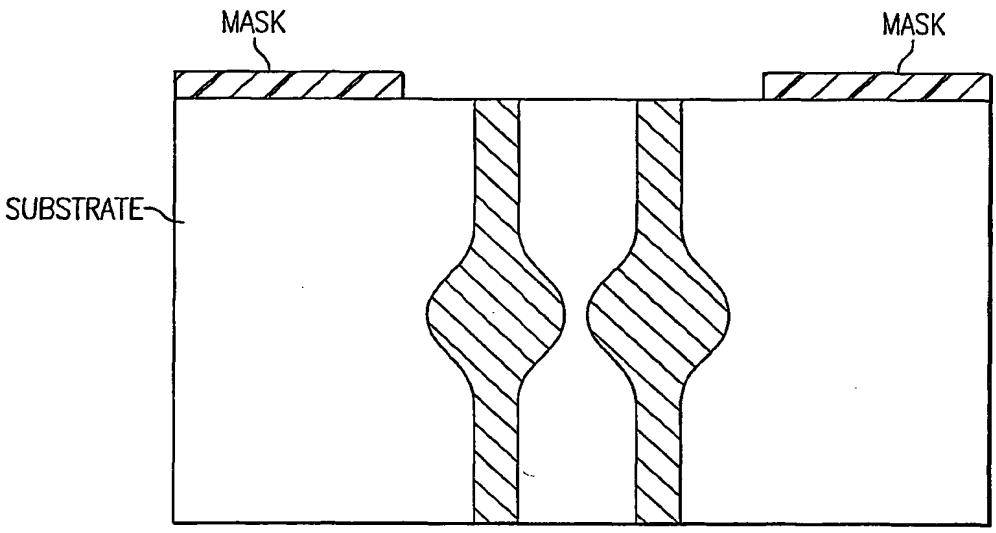

FIG. 13A

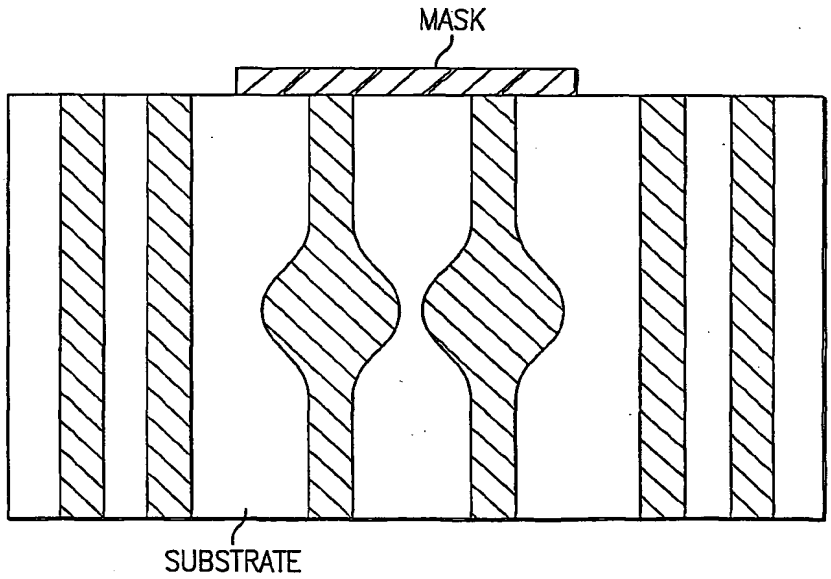

FIG. 13B

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(71) Applicant *(for all designated States except US)*: **XIDEX CORPORATION** [US/US]; 8906 Wall Street, Suite 105, Austin, TX 78754 (US).

(72) Inventor; and

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(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

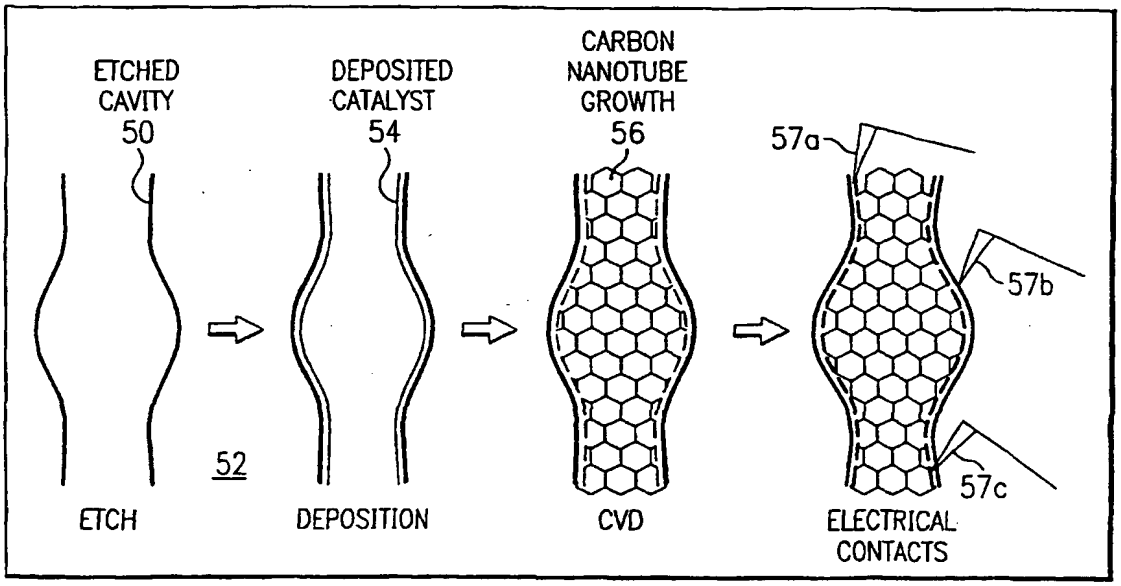
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

(88) Date of publication of the international search report:
3 January 2002

[Continued on next page]

(54) Title: SYSTEM AND METHOD FOR FABRICATING LOGIC DEVICES COMPRISING CARBON NANOTUBE TRANSISTORS



(57) Abstract: Carbon nanotube devices and methods for fabricating these devices, wherein in one embodiment, the fabrication process consists of the following process steps: (1) generation of a template, (2) catalyst deposition, and (3) nanotube synthesis within the template. In another embodiment, a carbon nanotube transistor comprises a carbon nanotube having two or more defects, wherein the defects divide the carbon nanotube into three regions having differing conductivities. The defects may be introduced by varying the diameter of a template in which the carbon nanotube is fabricated and thereby causing pentagon-heptagon pairs which form the defects.

WO 01/57917 A3

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INTERNATIONAL SEARCH REPORT

Inter ·ional Application No
PCT/US 01/04046

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L51/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
INSPEC, EPO-Internal, WPI Data, CHEM ABS Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 1995, no. 08, 29 September 1995 (1995-09-29) & JP 07 122198 A (NEC CORP), 12 May 1995 (1995-05-12) abstract ---	1,53,59
X	MENON M ET AL: "FULLERENE-DERIVED MOLECULAR ELECTRONIC DEVICES" SEMICONDUCTOR SCIENCE AND TECHNOLOGY, INSTITUTE OF PHYSICS. LONDON, GB, vol. 13, no. 8A, 1 August 1998 (1998-08-01), pages A51-A54, XP000768865 ISSN: 0268-1242 the whole document --- -/--	1,53,59

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
28 August 2001	04/09/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Königstein, C

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/04046

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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X	LI J ET AL: "HIGHLY-ORDERED CARBON NANOTUBE ARRAYS FOR ELECTRONICS APPLICATIONS" APPLIED PHYSICS LETTERS, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 75, no. 3, 19 July 1999 (1999-07-19), pages 367-369, XP000850812 ISSN: 0003-6951 the whole document	18,47
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INTERNATIONAL SEARCH REPORT

Inter onal Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	WO 01 03208 A (KIM KEVIN ;HARVARD COLLEGE (US); RUECKES THOMAS (US); JOSELEVICH E) 11 January 2001 (2001-01-11) the whole document	1

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter ional Application No
PCT/US 01/04046

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